AMENDMENTS TO THE CLAIMS

1-9 Canceled

10. (Amended) A method for storing a multi-bit value in a DRAM cell, the method comprising:

storing a charge in a cell capacitor, the stored charge producing one of a plurality of data voltage values;

precharging subbitlines of a pair of bitlines to one of a plurality of predetermined reference voltage levels;

dumping the stored charge onto a precharged subbitline of at least one pair of subbitlines to produce a sensing voltage;

determining a bit of the multi-bit value by comparing the sensing voltage to a reference voltage;

for each additional bit,

adjusting the reference voltage responsive to a last determined bit; and

determining the additional bit by comparing the sensing voltage to the adjusted reference voltage.

11. (Amended) The method of Claim 10, wherein adjusting the reference voltage comprises:

storing a charge in a dummy capacitor, said charge being indicative of previously determined bits;

charging at least one second cell capacitor to the reference voltage; and

dumping the charge stored in the dummy capacitor onto a plurality of subbitlines, and sharing said charge with the at least one second cell capacitor, the at least one second cell capacitor having a capacitance such that the adjusted reference voltage is established, said adjusted reference voltage being one of the plurality of predetermined reference voltage levels.

12. (Original) The method of Claim 10, wherein the pair of bitlines is divided into a number of subbitlines, said number responsive to the number of data voltage values.

13. (Amended) The method of Claim 10, wherein the DRAM cell is capable of operating in either of two modes, a first mode being a one bit per cell DRAM, and a second mode being a multibit per cell DRAM.

14. (Original) The method Claim 10, wherein adjusting the reference voltage is in the direction of a last sensed bit.

15. (Amended) A multi-bit DRAM cell, comprising:

a cell capacitor in which one of a plurality of data voltage values is maintained;

means for precharging subbitlines of a pair of bitlines, the pair of bitlines being subdivided into a plurality of subbitlines;

a plurality of switches for interconnecting the subbitlines;

a plurality of sensing amplifiers, each sensing amplifier associated with and switchably connected to a pair of subbitlines;

means for dumping a stored charge onto a precharged subbitline of at least one pair of subbitlines to produce a sensing voltage; and

means for adjusting a reference voltage responsive to a last determined bit.

16. (Amended) The multi-bit DRAM cell of Claim 15, wherein the switches are FET switches.

17. (Amended) The multi-bit DRAM cell of Claim 16, wherein the means for adjusting the reference voltage comprises:

a dummy capacitor, in which a charge indicative of previously determined bits is stored; and

at least one second cell capacitor having a capacitance such that upon dumping the charge stored in the dummy capacitor into said at least one second cell capacitor, the adjusted reference voltage is established, said adjusted reference voltage being one of a plurality of predetermined reference voltage levels.

18. (Original) The multi-bit DRAM cell of Claim 16, wherein the pair of bitlines is divided into a number of subbitlines, said number responsive to the number of data voltage values.

19. (Amended) The multi-bit DRAM cell of Claim 16, wherein the DRAM cell is capable of operating in either of two modes, a first mode being a one bit per cell DRAM, and a second mode being a multibit per cell DRAM.